The CompactPCI report

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Keying CompactPCI Backplanes and Boards

One reason behind CompactPCI's growing popularity is the high pin count that its 2mm connector technology provides. 3U boards have a total of 220 pins and 6U boards have a total of 535 pins. With all of these pins, you would think there would be enough to go around, but the increasing acceptance of the technology for a wide variety of applications is creating multiple definitions for all but the pins assigned to the core PCI bus itself.

Fortunately, both the 2mm connectors (as defined by the IEC 1076-4-101 spec) and the "new" Eurocard mechanics as defined by the IEEE 1101.10 Specification provided for methods of "keying" connectors and plug-in boards to prevent the mating of incompatible boards and backplanes. The PCI Industrial Computer Manufacturers Group (PICMG) is developing a central registry that accepts requests and grants allocations of keys for specific applications. The key assignments are being collated in a new PICMG spec, known as PICMG 2.1, which is currently under development.

3U CompactPCI boards (see Figure 1) and backplanes utilize two connectors with a total of 220 pins;

- J1 and J2 are the male backplane connectors,
- P1 and P2 are the female equivalents on a plug-in adapter board,
- J1/P1 provide 32-bit PCI connections and J2/P2 can be used for 64 bit PCI extensions, or for other sub-busses like National Instruments' PXI instrumentation bus, or for user I/O.

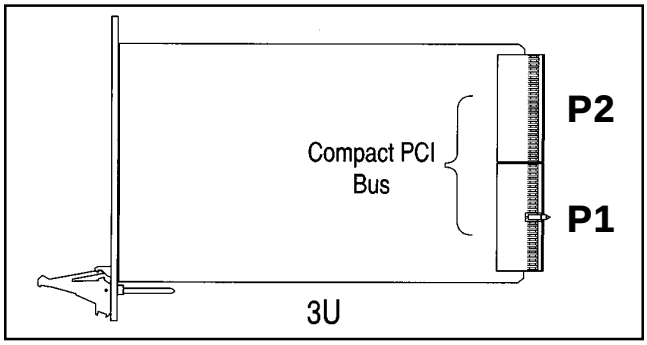

Figure 1

6U boards use the same two connectors at the bottom of the board and backplane (see Figure 2), but can accommodate up to three additional connectors (J3/J4/J5 on the backplane, P3/P4/P5 on an adapter board). These connectors can be used for sub-busses or I/O, leaving J1/P1 and J2/P2 for 64-bit PCI.

The 2mm connector technology as defined by the IEC 1076-4-101 spec provides for matching keying blocks in both male and female connector halves.

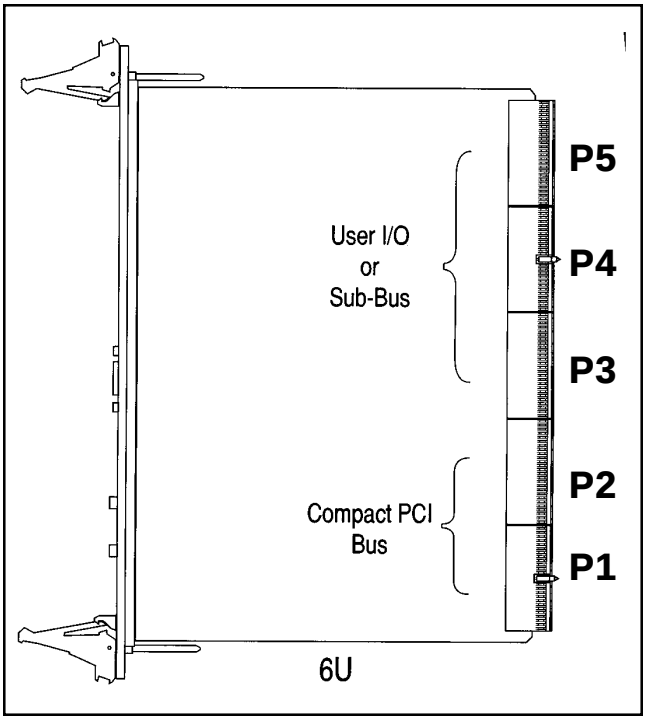

Figure 2

These connector keys are generally intended to prevent inadvertent installation of boards intended for a particular bus inter-connect in backplane slots intended for another. Only J1/P1 and J4/P4 on CompactPCI have these keys, and thus only these connectors are deemed to be protected by them.

IEC-1076 Connector Keys

The Type A connector specified in IEC 1076-4-101 includes provisions for installation of a keying block having eight coding positions. When installed this block is located in rows 12, 13, and 14 of the 25 row free and fixed connectors specified for J1/P1 and J4/P4.

In any given keying block, four coding positions are filled with blocking pins and four are left open to receive pins from the mating keying block. This arrangement allows for 70 mutually exclusive mating pairs, all of which are summarized in Annex D of IEC 1076-4-101. Figure 3 (*courtesy of ERNI Components*) illustrates the keying mechanism.

It is intended that a particular connector key will be uniquely associated with a particular use of the Type A connector regardless of the connector's position on the backplane.

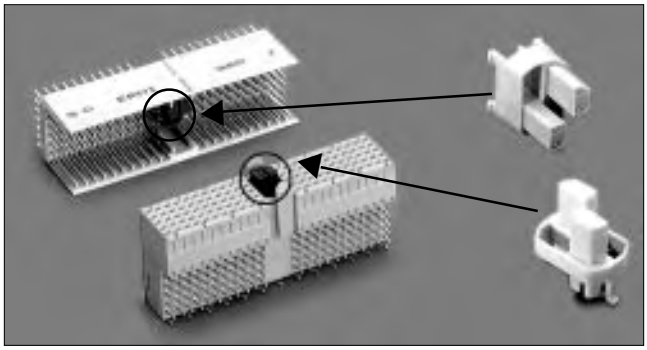

Figure 3

Ultimately, it is intended that seven of the 70 possible keying combinations will be identified as "User Defined," and the remainder which are unassigned reserved for future assignment.

The CompactPCI Base Specification has, in all revisions including the first, identified the "Brilliant Blue," RAL # 5007, J1/P1 key to signify 5.0 Volt signaling and the Cadmium Yellow, RAL # 1021, J1/P1 key to signify 3.3 Volt signaling on the CompactPCI bus. The absence of a J1/P1 key signifies universal (3.3V or 5V) signaling according to all specifications through Revision 2.1. When 64 bit extensions to PCI are implemented on J2/P2, the signaling levels are as indicated by the J1/P1 key.

The VME64 Extensions, as standardized under the auspices of VSO and ANSI, have been mapped onto J4/P4 and J5/P5 and the "Reseda Blue," RAL# 1021, key has been identified to signify that usage of the two connectors together.

The PICMG Telephony Subcommittee has requested the "Strawberry Red," RAL # 3018, key be used exclusively by the Computer Telephony (CT) industry for the purpose of preventing accidental insertion of any board that has P4 equipped, into a slot that has J4 wired per the CompactPCI Computer Telephony Specification for a CT sub-bus.

IEEE 1101.10 Front Panel Keys

The "new" Eurocard mechanics as defined by the IEEE 1101.10 specification includes more than just EMC gasketing and a new injector/ejector mechanism. The spec also specifies a front panel keying arrangement for 3U and 6U Eurocard boards.

The keying hardware includes two matching parts - the metal Eurocard-type front panel and a matching card guide located in the chassis. The back of the front panel butts up against the front of the chassis card guide. Each part incorporates three rectangular cavities. Each cavity can be fitted with an insert which fills half the cavity in any of four possible orientations. The mating key block on the front panel is fitted with pins of complementary orientation in each of the three positions. With three cavities and four positions in each, each mating block has 64 mutually exclusive combinations. Figure 4 (*courtesy of Rittal Corporation*) shows the bottom part of a front panel on the left, the front part of the card guide on the right, and the keying blocks in red. On 3U CompactPCI modules and enclosures, only one keying block, the "lower" block comprised of cavities D, E, and F, is installed so that only 64 combinations are available in 3U slots.

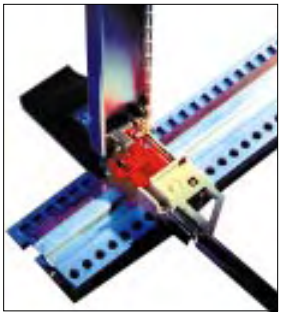

Figure 4

On 6U CompactPCI modules and enclosures an upper keying block, comprised of cavities A, B, and C, is installed in addition to the lower block yielding 4096 combinations.

In CompactPCI systems, J3/P3, J4/P4, and J5/P5 pins were originally identified as being user defined. The pins of J2/P2 are optionally available for user defined signals in 32 bit CompactPCI systems.

With the industry-wide acceptance of sub-bus definitions like the CompactPCI Computer Telephony Specification that use J4/P4 and J5/P5, there is a need to reserve front panel keys for each of these definitions and for user defined IO pins associated with the use of these sub-busses.

The majority of the 4096 available keying combinations be preserved for their original intended use - the differentiation of slot specific user defined IO functions. Only those keying combinations needed to protect bussed interconnects on J2/P2, J3/P3, and/or J5/P5 will be reserved.

It is worth noting that CompactPCI cards and backplanes that do not use 2mm connector pins for I/O or sub-busses need no keys at all. Furthermore, "universal" plug-in cards that can operate from 3.3V or 5V PCI buses need no IEC-1076 connector key, either.

Conclusion

To safely support overlapping uses of CompactPCI's user-definable pins, use of the keying mechanisms defined in IEC 1076-4-101 for the J1/P1 and J4/P4 connectors, and in IEEE 1101.10 for handle and card guide hardware are required. In the interest of providing a single reference document and to reduce the risk of duplicated use, assignment of these keys will be centrally administered by the PICMG Technical/ Executive Committee. A new PICMG specification (PICMG 2.1) is being developed to define the philosophy of their use and specific assignments.

Joe Pavlat is Director of Strategic Planning & Business Development for Motorola Computer Group. He is also President of the PCI Industrial Computer Manufacturers Group (PICMG), an industry consortium of over 360 companies dedicated to the development of open specifications using PCI technology for the industrial and telecommunications markets.